REMARKS

Claims 1-20 stand rejected under 35 USC §112, second paragraph. The Examiner cites Hann, U.S. patent 6,965,558, Brown et al. U.S. patent 6,778,526, James et al., U.S. patent 5,325,368 and Miura et al., U.S. patent publication US2004/0114509 as being pertinent to the present invention.

Claims 1, 5, 9, 10, 11, 14, 15, 16, 19 and 20 have been amended to more clearly state the invention. Reconsideration and withdrawal of the rejection under 35 USC §112, second paragraph of claims 1-20, as amended, is respectfully requested.

As amended, each of the independent claims 1, and 15, deletes and implementing enhanced fault tolerance and failure isolation features from the preamble, As amended, the apparatus of independent claim 1 is more clearly defined, now reciting a first interface coupled to a pair of master sources, a second interface coupled to a plurality of target interfaces, and a third interface coupled to a second controller for coupling a plurality of predefined controller control signals. As amended, the method of independent claim 15 is more clearly defined, now reciting connecting a third interface to a second controller for coupling a plurality of predefined control signals.

As amended, each of the dependent claims, the terms defining a master and resolving a master have been changed to controlling a master status. Such as in claim 5, as amended, recites a master control signal for controlling a master status for one of each of said pair of redundant selector functions and said pair of redundant ATTENTION monitor functions. Control of the master status of the redundant controller 130, 132 which include the pair of redundant selector functions and the pair of

redundant ATTENTION monitor functions is described at page 6 of the specification as follows:

In accordance with features of the preferred embodiment, each of the redundant controllers 130, 132 of the interface controller apparatus 100 feeds its MASTER status to the other controllers 130, 132 indicating that it is master and the other must not drive the system JTAG interfaces 104. If both are active, the PRIORITY signal, which is active only for one, is used to resolve to a single master. EXTMASTER allows an external source to assign the single master, though the MASTER function still resolves between two masters.

As amended, each of the claims 1-20, is believed to more clearly define the invention and to overcome the rejection under 35 USC §112, second paragraph. Withdrawal of the rejection under 35 USC §112, second paragraph of claims 1-20, as amended, is respectfully requested.

Hann, U.S. patent 6,965,558 discloses a method and system for protecting data transfers between a switch and physical network ports transfers data from a master network interface to a slave network interface, synchronizing the data transfer through a protection first in first out circuit that references the master clock and the slave clock. The master network interface improves ATM switch efficiency by supporting optical trunk and subtend ports for a digital subscriber line access multiplexer. The slave network interface provides back-up protection on a port basis so that a failed trunk port of the master network interface is backed up by the slave network interface even while the master network interface maintains a subtend port.

Brown et al. U.S. patent 6,778,526 discloses a high speed access bus interface for a communications network. The interface allows uni-directional transfer of data packets at a fast path processing rate of about 10 gigabits per second. The interface uses a master port and a slave port in a chip to chip data transfer scheme. The master and slave ports may have one or more than one data channel for transferring data packets. The master port includes a clock signal for synchronizing the transfer from the master port to the slave port. The slave may send an asynchronous signal to the master port in order to initiate the master port to stop or stall the pipeline transfer of data packets until space is made available in the slave port buffer. In addition to the clock synchronization, the interface utilizes an enable signal, a start of packet signal, an end of packet signal, an error signal (if necessary), a last valid byte signal, and a parity bit signal to identify, address, each data packet in the data stream. If a processing error occurs, the master port error signal to the slave port also initiates the slave port to disregard the previous data packet. The operating frequency of 50 MHz allows the data packet transfer to exceed 10 gigabits per second.

James et al., U.S. patent 5,325,368 discloses nonvolatile memory that is provided on each module of a computer system including one or more modules with each module including a plurality of components including JTAG technology. A test bus operable in accordance with the 1149.1 standard is included in the computer system and is arranged to access the nonvolatile memory. Boundary scan information for the components on a module and also additional information, preferably fully describing all JTAG related characteristics and operations, is stored in the nonvolatile memory. A

JTAG bus system is then able to access the module memory and obtain all information required to fully implement JTAG operations for the module.

Miura et al., U.S. patent publication US2004/0114509 discloses a multiplexing control system has a common process input/output unit for distributing process signals from sensors for measuring the same state variable of a process to digital controllers. One process input/output unit for inputting/outputting a process signal between the multiplexing control system and plant is provided for each process signal. The process input/output unit for the process signal of high importance is triplexed. A process controller having an operating function is provided to each of the triplexed process input/output units. A process input/output unit for the process signal of intermediate importance is diplexed. A process input/output unit for the process signal of low importance is monoplexed. The process signals of the diplexed process input/output units and the monoplexed process input/output unit are controlled by a controller having a master right among the process controllers.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention as recited in each of the claims 1-20, as amended, is patentable over all the art of record.

Applicants respectfully submit that apparatus and method for customizing and monitoring multiple interfaces as respectively recited in independent claims 1 and 15, as amended, are neither disclosed, nor suggested by the total teaching of the Hann, Brown et al., James et al., and Miura et al. references. Applicants respectfully submit that the first, second and third interfaces, first multiplexer, pair of second multiplexers,

and pair of redundant selector functions, and pair of redundant ATTENTION monitor functions, as recited in independent claims 1 and 15, as amended, are neither disclosed, nor suggested by the total teaching of the Hann, Brown et al., James et al., and Miura et al. references.

Thus, independent claims 1 and 15, as amended, are patentable.

Dependent claims 2-14, and 16-20, further define the invention of patentable independent claims 1 and 15, as amended, and are likewise patentable.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-20, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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